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(54) DYNAMIC RAM

(57) Abstract:

PURPOSE: To improve the operation margin by providing a voltage supply circuit at each sense amplifier circuit, dividing the circuit into plural sense amplifier circuit groups operated at the same time and connecting them to a common power wiring or ground wiring.

CONSTITUTION: A sense amplifier circuit relating to a memory array M-ARY is divided into two sense amplifier circuit groups SAG1, SAG2, the timing signals ϕpa12 and ϕpa12 are supplied to the 2nd sense amplifier circuit group and similar read operation is executed. The sense amplifier circuit groups SAG1, SAG2 are connected to a common grounding line GND on a semiconductor chip, the amplifier is operated individually by the address selection or both the sense amplifier circuit groups are not simultaneously operated by giving a slight timewise difference to timing signals ϕpa11, ϕpa21 and ϕpa12, ϕpa22. Thus, the voltage fluctuation or noise is less, the operation margin is improved and a dynamic RAM suitable for large capacity is realized.

DYNAMIC RAM

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(54) DYNAMIC RAM

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Specification

Title of Invention

DYNAMIC RAM

Scope of Patent Claim

1. A dynamic RAM, which is characterized by the fact that it comprises unit circuits made from amplification MOSFETs where the input-output nodes are joined to the data lines comprising the memory array, sense amplifiers made from switch MOSFETs that are set up for each of the aforementioned unit circuits and supply operating voltage to the circuits, and a timing control circuit. The unit circuits comprising the aforementioned sense amplifiers are divided into several groups and the timing control circuit supplies several types of operation timing signals that correspond to the respective group of unit circuits to the aforementioned switch MOSFETs.

2. The dynamic RAM in claim 1, which is characterized by the fact that the aforementioned several groups of unit circuits are individually selected one group at a time and are not simultaneously selected.

3. The dynamic RAM in claim 1, which is characterized by the fact that the aforementioned several groups of unit circuits are simulatneously selected and operated based on a very small time difference by timing signals with a very small time difference that have been supplied from the aforementioned timing control circuit.

4. The dynamic RAM in claim 1, which is characterized by the fact that the aforementioned unit circuits are 2 sets that are placed (illegible) symmetrically with respect to the operating voltage line.

Detailed Description of Invention

[Technological field]

The present invention pertains to a dynamic RAM (random access memory). It pertains to technology that is useful in dynamic RAMs having, for instance, several sense amplifier circuits that operate simultaneously.

[Prior art]

Sense amplifier circuits are used in dynamic RAMs to read the stored data in the memory cells, and the sense amplifier circuits, the number of which corresponds to the command of one word line (row address), are simultaneously brought to an operating state In the past, these groups of sense amplifier circuits that are simultaneously brought to an operating state have been connected to common power source voltage supply circuits.

The signals for reading stored data to be input in each of the sense amplifiers are very small signals, depending on whether or not there is (illegible) that has accumulated in the capacitor for data storage of the memory cells, and therefore, when the sense amplifier circuits are designed with high density, operation timing becomes inflexible as well.

The number of sense amplifier circuits that operate simultaneously increases with an increase in integration and capacity of the RAM and therefore, the overall operating current increases. Consequently, the problems have arisen of a reduction in the operating margin and a delay in the operating speed of the sense amplifier circuits due to changes in the operating voltage resulting from the resistance component of the wiring that supplies the power-source voltage or ground potential to these sense amplifier circuit groups, as well as the noise to other circuits that accompanies disconnection of a relatively large operating current to the sense amplifier circuit groups, etc. (refer to, for instance, Japanese Kokai Patent No. Sho 53(1978)-66,130 for sense amplifier circuits).

[Purpose of invention]

The purpose of the present invention is to present a dynamic RAM that has an improved operating margin and that is suitable for increasing capacity, but has a simple structure.

The aforementioned objective, as well as other purposes and new characteristics of the present invention will be clarified by the following description and figures.

[Summary of invention]

The following is a brief description of an example of the invention disclosed in the present application: That is, voltage supply circuits that supply operating current to the sense amplifier circuits are set up for each sense

amplifier circuit, and the sense amplifiers circuits are divided into several groups of sense amplifiers that are simultaneously brought to an operating state. The groups of sense amplifiers that do not simultaneously operate are connected to a common electrical source line or ground line spatially by an appropriate layout or temporally by timing signals. As a result, the operating current of the sense amplifier circuits that passes through the power-source line or the ground line is reduced and the operating margin of the RAM is improved and speed is increased.

[Examples]

Figure 1 is a circuit diagram of an example of the dynamic RAM of the present invention. Although there are no special restrictions, each circuit element or circuit block in the same figure is formed in one semiconductor substrate of, for instance, single crystal silicon by conventional technology for producing semiconductor integrated circuits.

One-bit memory cell MC comprises MOSFET Qm for address selection and data storage capacitor C_s, where one electrode is connected to Qm and the other electrode is kept at the power-source voltage level of the circuit. Data of logic "1", "0" is stored in the form of : "Is there or is there not a charge at capacitor C_s?".

Data are read by turning MOSFET Qm on and connecting capacitor C_s to common data line DL and sensing what changes in the potential of data line DL will occur in accordance with the charge that has accumulated at capacitor C_s.

Although there are no special restrictions, dummy cell DC is set up as the reference for detecting this very small signal. (illegible) the capacity of this capacitor Cd is approximately half the capacity of capacitor C_s of memory cell MC. this dummy cell DC is made under the same production conditions and with the same design constants as memory cell MC. Capacitor Cd is set (discharged) before addressing by MOSFET Qd, which receives timing signal ϕd. As previously explained, capacitor Cd is designed so that its capacity is approximately half that of capacitor C_s and therefore, a reference voltage equal to approximately half the read signals from memory cell MC is formed.

The USA in the same figure is a unit circuit of a sens amp where the difference in this potential change produced by the aforementioned addressing spreads to the sense period determined with timing signal (sense control signal) ϕpa. Its input-putput node is connected to complementary data lines DL and $\overline{DL}$, which are a parallel pair. This sense amp USA has MOSFETs Q1 and Q2, which are a cross-connected pair, and very small signals that have emerged in complementary data lines DL and $\overline{DL}$ are differentially amplified by the positive feedback effect of these MOSFETs. Moreover, this positive feedback operation is performed in 2 steps by MOSFETs Q7 and Q8, whose drains are connected to the source of MOSFET Q1 and Q2. That is, MOSFETs Q7, which has been designed for a relatively low conductance, is started by relatively fast timing signals ϕpa11 and the positive feedback operation simultaneously starts. The

high-level data line potential falls at a slow speed while the low-level data line potential falls at a fast speed, with their difference becoming larger, based on the potential difference applied to complementary data lines DL and $\overline{DL}$ with addressing. At this time, MOSFET Q8, which has been designed for a relatively high conductance, is started by timing signal ϕpa11 by timing that is not as great as the aforementioned difference in potential and therefore, the aforementioned low level data line potential suddenly decreases. Thus, the aforementioned high level potential is kept from caving in by operation of the sense amplifier circuit USA in 2 steps. Therefore, when the low-level potential falls below the threshold voltage of the cross-connected MOSFETs, positive feedback operations stop. The drop in the high-level potential stops at a potential that is lower than the power source voltage Vcc and higher than the aforementioned threshold voltage, and the low-level potential eventually reaches the ground potential (0 V).

The number of memory cells joined to each complementary data line $\overline{DL}$ and DL is the same in order to improve detection reliability. One dummy cell is connected to each of complementary data lines DL and $\overline{DL}$. Moreover, each memory cell MC is joined between one word line WL and the pair of complementary data lines. Each word line WL intersects with both pairs of data lines and consequently, the noise component applied to each data line by the unnecessary combined capacity when the potential of word line WL changes

becomes common mode noise and is essentially offset by differential sense amplifier USA.

By means of the present example, the sense amplifier circuit related to this memory array M-ARY is divided into two groups, sense amplifier circuit group SAG1 and group SAG2, and timing signals ϕpa12 and ϕpa22 are supplied to the second sense amplifier circuit group and the same reading operation is performed. As will be mentioned later, these sense amplifier circuit groups SAG1 and SAG2 are connected to a common ground line on the semiconductor chip and are either individually brought to an operating state by address selection, or both sense amplifier circuit groups are simultaneously brought to an operating state by applying a very small time lag to timing signals ϕpa11 and ϕpa21 as well as ϕpa12 and ϕpa22.

However, as a result of addressing, when memory cell MC connected to one of the pair of complementary data lines DL and $\overline{DL}$ is selected, one of a pair of dummy word lines DWL and $\overline{DWL}$ is selected so that dummy cell DC will always be connected to the other data line.

In the case of the aforementioned addressing, the stored data of memory cell MC, which were once destroyed, are recovered by retrieving the high-level or low-level potential obtained by this sense operation. Nevertheless, if the high level caves in by a certain amount or more with respect to power-source voltage Vcc, malfunctioning occurs when the result is read as logic "0", while repeating reading and rewriting several times In order to prevent this malfunction, active

restore circuit AR is used. By means of this active restore circuit AR, timing signals ϕrs selectively boost (raise) only the high-level signals to the potential of the power-source voltage Vcc without having any effect on the low-level signals.

Data line pair DL and $\overline{DL}$, which are shown in the same figure, are selectively joined to common complementary data line pair CDL and $\overline{CDL}$ by column switch CW. That is, column switch MOSFETs Q3 and Q4, which are controlled by the output of column decoder D-CDR, are placed between aforementioned complementary data lines DL and $\overline{DL}$ and common complementary data line pair CDL and $\overline{CDL}$. The data line pairs in another example are also connected to common complementary data line pairs CDL and $\overline{CDL}$ by MOSFETs Q5 and Q6.

Aforementioned common complementary data line pairs CDL and $\overline{CDL}$ are connected to the input terminal of data output buffer DOB, which has an output amp, and the output terminal of data input buffer DIB. The input terminal of aforementioned data input buffer DIB is connected to outside terminal Din, which supplies the write data. The output terminal of aforementioned data output buffer DOB is connected to outside terminal Dout, which transmits the read data.

There are no special restrictions to aforementioned data input buffer DIB and data output buffer DOB, but they are made from CMOS static circuits. Data

input buffer DIB is brought to an operating state during writing operations by timing signal ϕrw and transmits writing signals that have been supplied from outside terminal Din to common complementary line pairs CDL and $\overline{\text{CDL}}$ when in this operating state. Moreover, if reading operations are being performed, the output of data input buffer DIB is brought to a state of high impedance by aforementioned timing signals ϕrw. While in this operating state, read data signals are sent from outside terminal Dout.

Row decoder R-DCR and column decoder C-DCR receive internal complementary address signals formed by row adress buffer R-ADB and column address buffer C-ADB. One word line and a dummy word line, as well as column switch selection signals, are formed and addressing of the memory cell and the dummy cell is performed That is, row address buffer R-ADB is brought to an operating state by timing signals ϕ are formed by row address strobe signals $\overline{\text{RAS}}$. Address signals AX0-AX1, which have been fed from the outside terminal in synchronization with the aforementioned row address strobe signals $\overline{\text{RAS}}$, are incorporated and stored as they are transmitted to row decoder R-DCR while in this operating state. Row decoder R-DCR decodes the aforementioned address signals that have been transmitted and specific word lines and dummy word lines in accordance with the aforementioned address decoder output are selected by word line selection timing signals ϕx.

Moreover, although there are no special restrictions, column address buffer C-ADB is made from CMOS static circuits. Its operation is controlled by timing signals ϕac, which are formed by column address strobe signals $\overline{CAS}$, and they receive address signals AY0-AYi fed from the outside. Internal complementary address signals formed by column address buffer C-ADB are sent to column decoder C-DCR, which is similarly made from CMOS static circuits. Column decoder C-DCR is controlled by data line selection timing signals ϕy and decodes address signals that have been transmitted to it and selects data lines in synchronization with data line selection timing signals ϕy.

Timing control circuit TC receives row address strobe signals $\overline{RAS}$, column address strobe signals $\overline{CAS}$ and write enable signals $\overline{WE}$, which have been supplied an outside terminal, and forms timing signals, such as those described above, as well as other types of timing signals necessary for memory operation.

The circuit diagram is an example of the state in which the aforementioned two groups of sense amplifiers and ground line GND are connected. In the figure, sense amplifier circuit group SAG1, which is made from unit sense amplifier circuits US11-US1m, and second sense amplifier circuit group SAG2, which is made from unit sense amplifier circuits US21-US2m, are lined up in a row on one side of ground line GND. The unit sense amplifier circuits of first sense amplifier circuit group SAG1 are made from a differential

amp, which comprises cross-connected MOSFETs Q111-Q11m and Q211-Q21m corresponding to MOSFETs Q1 and Q2 in Figure 1, and a ground potential feed circuit, which comprises parallel-connected MOSFETs Q711-Q71m and Q811-Q81m corresponding to MOSFETS Q7 and Q8 in Figure 1. The gates of MOSFET Q711 - Q71m are connected together and timing signals ϕpa11 are supplied, while timing signals ϕ21, which are somewhat slower than timing signals ϕpa11, are supplied to the gates of MOSFETs Q811 - Q81m.

On the other hand, second sense amplifier circuit group SAG2 has the same structure as that of the first sense amplifier circuit group and each of its ground-potential supply circuits is operated by common timing signals ϕpa12 and ϕpa22 . Timing signals ϕpa12 and ϕpa22 of the second sense amplifier circuit group are somewhat slower than timing signals ϕpa11 and ϕpa21 of the first sense amplifier circuit group. Second sense amplifier circuit group SAG2 is brought to an operating state somewhat later than first sense amplifier circuit group SAG1.

Figure 4 shows operation timing during reading operations of the aforementioned dynamic RAM. In the figure, X address signals AX0-AX1, which are multi-address signals supplied from the outside, are incorporated in timing signals ϕar formed by the rise timing of row address strobe signals $\overline{RAS}$ and sent to row decoder R-DCR. Row decoder R-DCR brings a word line that has been assigned to the X address signals by timing signals ϕx, which are somewhat slower than timing signals ϕar, to the selected state. Next, unit sense

amplifier circuits USA11 -USA1m in first sense amplifier circuit group SAG1 simultaneously perform the second step of reading operations with timing signals ϕpa11 and ϕpa21 and unit sense amplifier circuits USA21 - USA2m in slightly delayed second sense amplifier circuit group SAG2 similarly simultaneously perform the second step of reading operations with timing signals ϕpa21 and ϕpa22. Y address signals AY0–AY^{i}, which are multi-address signals supplied from the outside, are incoprorated in column address buffer C-ADB by timing signals ϕac formed by the rise timing of column address strobe signals $\overline{\text{CAS}}$ and are sent to column decoder C-DCR. Column decoder c-DCR (illegible) the gate of the one data line assigned to the Y address by timing signals ϕy. which are somewhat delayed in comparison to timing signals ϕac. and read data are output from the memory.

However, the current consumed in the aforementioned sense amplifier circuit groups accumulates during the relatively short period of time until each sense amplifier circuit has completed evaluation of the read data from the memory cell. A temporary increase in the current by the same operation can be cut approximately in half by applying a time lag to the time when the two sense amplifier circuit groups begin operating, as in the present example. Therefore, the current flowing through ground line GND when the sense amplifier circuits are operating can be cut approximately in half and as a result, voltage fluctuations can be reduced and the operating margin can be improved, and high-speed operation becomes possible.

On the other hand, in the case of the present example, the access time of the entire RAM is long because second sense amplifier circuit group SAG2 operates somewhat slower than first sense amplifier circuit group SAG1, but this problem can be solved by selecting with the 2 sense amplifier circuit groups under different selection conditions. For instance, a dynamic RAM performs rewriting by a refresh operation at a certain time interval in order to retain the stored data. Therefore, it has a memory array that performs reading and a memory array for refresh operations, even during normal reading operations. In this case, access time can be curtailed by using timing signals ϕpa11 and ϕpa21 shown in Figure 4 for the memory array that reads and timing signals ϕpa12 and ϕpa22 for the memory array that performs the refresh function.

Figure 3 is the circuit diagram of another example of the state of connection of the two sense amplifier circuit groups and ground line GND. In the figure, the summary of each circuit element comprising the circuit and their operation is the same as in aforementioned Figure 2. First sense amplifier circuit group SAG1 and second sense amplifier circuit group SAG2 are laid out in a symmetric manner sandwiching ground line GND. Therefore, in addition to the results in the example in aforementioned Figure 2, there is an advantage in that the width of ground line GND can be increased That is, for instance, by constructing the switch MOSFETs for the voltage supply circuits of the two sense amplifier circuits SAG1 and SAG2 on the bottom layer with respect to the ground line GND, which is wired with an aluminum layer on a semiconductor chip, etc.,

the width of the aluminum layer on ground line GND can be increased, that is, resistance of the ground line can be reduced, etc., and a high-speed dynamic RAM with few voltage fluctuations and little noise can be produced.

(Results)

(1) The sense amplifier circuits are divided into several sense amplifier circuit groups and are laid out relative to a common power line or ground line using a spatial or a timing pattern that does not allow these sense amplifier circuit groups to be brought to an operating state simultaneously. As a result, the current that flows to the power line or ground line when the sense amplifier circuits are operating is reduced and a dynamic RAM that has few voltage fluctuations and little noise and an improved operating margin, and which is suitable for high capacity, is produced.

(2) The wiring of an aluminum layer, etc., on the ground line can be spread out by arranging the sense amplifier groups symmetrically sandwiching the ground line on a semiconductor chip, and as a result, the ground line resistance is reduced and a dynamic RAM with an even better operating margin can be produced

The present invention was explained based on examples, but this invention is not restricted to these examples and it goes without saying that various alterations can be made as long as the essential points remain unchanged. For instance, there are various embodiments possible for the dividing the sense amplifier circuit groups. The voltage supply circuits of the

sense amplifier circuits are not necessarily set up for each sense amplifier circuit and a common voltage supply circuit can be used for several sense amplifier circuits. Moreover, a volgate supply circuit can be set up for both the power-source voltage and the ground potential of the sense amplifiers, or the power-source line and the ground line can be used with the same layout as previously described, when making the sense amplifier circuits from the CMOSs (complementary MOSs).

(Fields of application)

The present invention can be used for a wide variety of dynamic RAMs that have several sense amplifier circuits

Figure 1 is an example of the dynamic RAM of the present invention;

Figure 2 is a circuit diagran showing an example of the state of connection of the sense amplifier circuit groups and ground line in Figure 1;

Figure 3 is a circuit diagram of another example of the state of connection of the sense amplifier circuit groups and ground line in Figure 1; and

Figure 4 is a diagram of the operation timing of the dynamic RAM in Figure 1

MC. memory cell

DC. dummy cell

CW. column switch

SA. sense amplifier

M-ARY. memory array

AR active restore circuit

R-DCR. row decorder

C-DCR. column decoder

R-ADB row address buffer

C-ADB. column address buffer

DOB. data output buffer

DIB. data iniput buffer

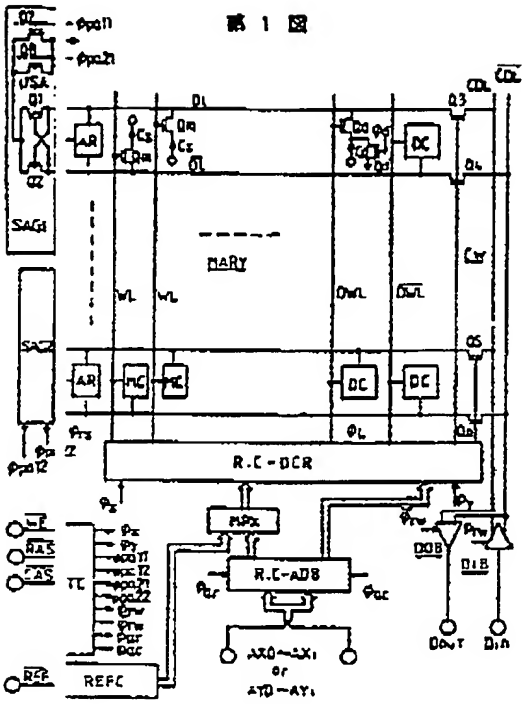
TC. timing control circuit

SAG1, SAG2. sense amplifier circuit groups

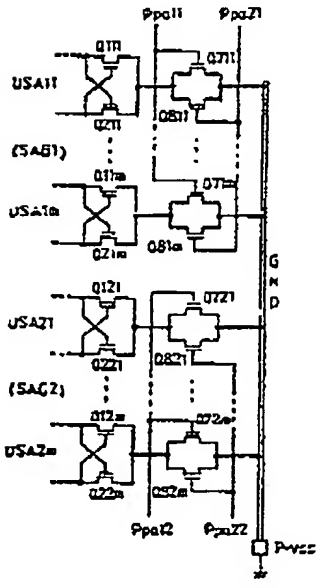
USA11 - USA1m, USA21 - USA2m. unit sense amplifier circuits

GND ground line

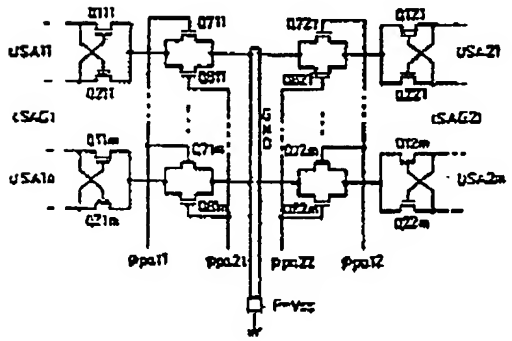
第 1 図



第 2 図



第 3 図



第 4 図